CLAIMS

1. A semiconductor device including at least one p-channel type MOS transistor, which device comprises:

a semiconductor substrate;

a gate insulating layer formed on said semiconductor substrate; and

a gate electrode formed on said gate insulating layer, said gate electrode having a multi-layered structure including a silicon-seed layer formed as a lowermost layer on said gate insulating layer, a polycrystalline silicon layer formed as an uppermost layer above said lowermost layer, and a silicon/germanium layer formed as an intermediate layer between said lowermost and uppermost layers,

wherein an average grain size of polycrystalline silicon in said uppermost layer being at most 100 nm, p-type impurities are substantially uniformly distributed in said gate electrode along a height thereof, and the germanium atoms are diffused from said intermediate layer into said lowermost layer at high density.

2. A semiconductor device as set forth in claim 1, wherein said lowermost, intermediate, and uppermost layers are formed by using a chemical vapor deposition method, and the formation of said uppermost layer is carried out at a higher process temperature than a process temperature at which said lowermost and intermediate layers are formed.

3. A semiconductor device as set forth in claim 2, wherein said chemical vapor deposition method is performed by a leaf-type chemical vapor deposition apparatus, the formation of said lowermost and intermediate layers is carried out at a process temperature falling a range between approximately 550°C and approximately 650°C, and the formation of said uppermost layer is carried out at a process

temperature falling in a range between approximately 680°C and approximately 800°C.

4. A semiconductor device as set forth in claim 2, wherein said chemical vapor deposition method is performed by a batch-type chemical vapor deposition apparatus, the formation of said lowermost and intermediate layers is carried out at a process temperature falling a range between approximately 450°C and approximately 550°C, and the formation of said uppermost layer is carried out at a process temperature falling in a range between approximately 600°C and approximately 650°C.

5. A semiconductor device as set forth in claim 2, wherein said p-type impurities are implanted in said gate electrode, and the uniform distribution of said p-type impurities in said gate electrode and the diffusion of the germanium atoms from said intermediate layer into said lowermost are simultaneously achieved by annealing said semiconductor substrate at a higher process temperature than the process temperature at which said lowermost and intermediate layers are formed.

6. A production process for manufacturing a semiconductor device including at least one p-channel type MOS transistor, which process comprises:

preparing a semiconductor device;

forming a gate insulating layer on said semiconductor substrate;

forming a gate electrode on said gate insulating layer, said gate electrode having a multi-layered structure including a silicon-seed layer formed as a lowermost layer on said gate insulating layer, a polycrystalline silicon layer formed as an uppermost layer above said lowermost layer, and a silicon/germanium layer formed as an intermediate layer between said lowermost and uppermost layers, the formation of

said uppermost layer being carried out at a higher process temperature than a process temperature at which said lowermost and intermediate layers are formed;

implanting p-type impurities in said gate electrode; and

annealing said semiconductor substrate at a higher process temperature than the process temperature at which said uppermost layer is formed, such that said p-type impurities are substantially uniformly distributed in said gate electrode along a height thereof, and the germanium atoms are diffused from said intermediate layer into said lowermost layer at high density.

7. A production process as set forth in claim 6, wherein the formation of said lowermost, intermediate, and uppermost layers is carried out by using a chemical vapor deposition method.

8. A production process as set forth in claim 7, wherein said chemical vapor deposition method is performed by a leaf-type chemical vapor deposition apparatus, the formation of said lowermost and intermediate layers is carried out at a process temperature falling a range between approximately 550°C and approximately 650°C, and the formation of said uppermost layer is carried out at a process temperature falling in a range between approximately 680°C and approximately 800°C.

9. A production process as set forth in claim 7, wherein said chemical vapor deposition method is performed by a batch-type chemical vapor deposition apparatus, the formation of said lowermost and intermediate layers is carried out at a process temperature falling a range between approximately 450°C and approximately 550°C, and the formation of said uppermost layer is carried out at a process temperature falling in a range between approximately 600°C and

approximately 650°C.

10. A production process as set forth in claim 6, wherein both a p-type drain-formation region and a p-type source-formation region are defined in said semiconductor substrate while implanting said p-type impurities in said gate electrode, and the respective p-type drain-formation and p-type source-formation regions are produced as a drain region and a source region while annealing said semiconductor substrate at the higher process temperature than the process temperature at which said uppermost layer is formed.

11. A production process as set forth in claim 6, further comprising forming an insulating side wall around said gate electrode, wherein the formation of said insulating side wall is performed prior to the annealing of said semiconductor substrate

12. A production process as set forth in claim 6, further comprising forming an insulating side wall around said gate electrode, wherein the formation of said insulating side wall is performed after the annealing of said semiconductor substrate.